In the Specification

Amend the following numbered paragraphs of the specification:

[0005] The performance requirements of divider circuits have increasingly demanded a greater number of divide modes, a wider divide range, and the smallest possible divide resolution. There are currently many divider styles in use that address each of these requirements individually. The real challenge, however, is to meet ~~these~~ all of these requirements along with the additional demands that a divider circuit be able to process higher signal frequencies, occupy less physical area and consume less power.

[0032] Fig. 17 depicts a frequency divider circuit wherein the symmetrical divider of Fig. 16 is replaced with a symmetrical divide-by-four component.

[0039] Fig. 24 ~~depicts the state transition table for LFSR of Fig. 23~~ shows an eight latch LFSR with a multistage XOR feedback network distributed across multiple latches.

[0040] Fig. 25 ~~shows an eight latch LFSR with a multistage XOR feedback network distributed across multiple latches~~ depicts the state transition table for LFSR of Figs. 23 and 24.

[0086] Because the logical XOR is distributed across two clock cycles, it is possible that the latch L0 will not reflect the value it would have had in the original single cycle feedback network of Fig. 23. With the modified feedback structure, latch L0 will now occasionally contain a known "false" value that will be corrected during the next clock cycle via the XOR 204 between latches L0 and L1 in Fig. ~~25~~ 24. The table 206 in Fig. 26 illustrates the progression of several LFSR states. These same states are listed in the table of Fig. ~~24~~ 25.

[0096] A fifth embodiment of the high speed LFSR counter of the frequency divider, shown in Fig. 34, adds an additional programmability feature by providing a multiplexed input to each of the LFSR latches. The LFSR counter latches can be initialized to specific values via a latch RESET

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